UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/754,726	01/12/2004	Chao-Hsin Lu	LUCH3011/EM	1341

27765 7590 11/30/2006

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
NGUYEN, LONG T	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 11/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/754,726	LU, CHAO-HSIN	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *24-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *24-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 30-37 are objected to because of the following informalities:

Claim 30, line 3, "the at least one of" should be changed to --at least one of--.

Claim 31 is objected to because it includes the informality of claim 30.

Claim 32, line 7, "the at least one of" should be changed to --at least one of--.

Claim 33-37 are objected to because they include the informality of claim 32.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 24-43 are rejected under 35 U.S.C. 102(e) as being anticipated by Dillon (USP 6,700,403).

With respect to claim 24-27 and 30-37, Figure 2 shows a driving apparatus, which includes: an output circuit (transistors 71 and 72 in both 65 and 66) to output a different signal (PAD1, PAD2), a reference current control circuit (whichever circuit that is used to generated D1, D2) to provide a control voltage (D1, D2), a switch circuit (91, 92 and inverters 73 and 74 for both 65 and 66, also see Col. 4, lines 11-18) coupled to the output circuit and to the reference current control circuit for selectively applying the control voltage (D1, D2), an operational

voltage (Vdd) and ground to the output circuit; wherein a magnitude of the differential signal (PAD1, PAD2) is determined based on at least one of a difference of the operational voltage and a first control voltage of the control voltage (Vdd and D1), and a difference of the control voltage and ground (D2 and ground). Note that "to output a differential signal" is merely a function intended use limitation and the circuit in Figure 2 of Dillon is fully capable of generates a differential output signal because the circuit in Figure 2 is fully capable of receiving any signal its inputs including a differential input signal (D1, D2) and when receiving a differential input signal at its inputs (D1, D2), then the circuit will generate a differential output signal, i.e., the output signals (PAD1, PAD2) are differential signals. Note that Dillon also discloses that in successive response to Vdd and ground signals from the multiplex 70, successive output signals at output ports 21 and 22 will have substantially Vdd and ground signal levels (Col. 3, lines 37-42), so the signals at ports 21 and 22 are also differential signal. Furthermore, it is also note that the output circuit (transistors 71 and 72 in both 65 and 66) comprises a first transistor (PMOS 71 in 65), a second transistor (NMOS 72 in 65), a third transistor (PMOS 71 in 66) and a fourth transistor (NMOS 72 in 66); wherein while the first and fourth transistors are ON then the second and third transistors are OFF and vice versa, and while the output circuit output circuit outputs the different signals, at least one of the first, second, third and fourth transistors operates at a saturation region (inherently because when the transistor is fully ON then it operates at saturation region).

With respect to claims 28 and 29, Figure 2 shows that the output circuit (transistors 71 and 72 in both 65 and 66) comprises a first transistor (71 in 65), a second transistor (72 in 65), a third transistor (71 in 66) and a fourth transistor (72 in 66); and wherein the switch circuit (91, 92

and inverters 73 and 74 for both 65 and 66, also see Col. 4, lines 11-18) comprises a first switch (97 in 91), a second switch (97 in 92), a third switch (98 in 91), a fourth switch (98 in 92), a fifth switch (95 in 91 with inverter 73 in 65), a sixth switch (96 in 91 with inverter 74 in 65), a seventh switch (95 in 92 with inverter 73 in 66), and an eighth switch (96 in 92 with inverter 74 in 66). Note that, in Figure 2 of Dillon, a first control voltage signal (D1), a second voltage control signal (D2), and it is inherent that there must be a switch control circuit to control the switches in Figure 2 of Dillon.

With respect to claims 38-43, Figure 2 of Dillon shows the output circuit (transistors 71 and 72 in both 65 and 66) for outputting a differential signal (PAD1, PAD2) comprising a first transistor (PMOS 71 in 65), a second transistor (NMOS 72 in 65), a third transistor (PMOS 71 in 66) and a fourth transistor (NMOS 72 in 66), a first control signal (D1), a second control signal (D2), a third control signal (Vdd), and a fourth control signal (ground). Note that "to output a differential signal" is merely a function intended use limitation and the circuit in Figure 2 of Dillon is fully capable of generates a differential output signal because the circuit in Figure 2 is fully capable of receiving any signal its inputs including a differential input signal (D1, D2) and when receiving a differential input signal at its inputs (D1, D2), then the circuit will generate a differential output signal, i.e., the output signals (PAD1, PAD2) are differential signals. Note that Dillon also discloses that in successive response to Vdd and ground signals from the multiplex 70, successive output signals at output ports 21 and 22 will have substantially Vdd and ground signal levels (Col. 3, lines 37-42), so the signals at ports 21 and 22 are also differential signal. Furthermore, it is also note that a magnitude of the differential signal is determined based on at least one of a difference of the third control voltage and the first control voltage (Vdd and

D1), and a difference of the second control voltage and the fourth control voltage (D2 and ground). Also, note that, while the output circuit output circuit outputs the different signals, at least one of the first, second, third and fourth transistors operates at a saturation region (inherently because when the transistor is fully ON then it operates at saturation region).

Response to Arguments

4. Applicant's arguments filed on 10/3/06 have been fully considered but they are not persuasive.

Applicant argues that the circuits 65 and 66 of Dillon cannot output a differential signal. However, this argument is not persuasive because "to output a differential signal" is merely a function intended use limitation and the circuit in Figure 2 of Dillon is fully capable of generates a differential output signal because the circuit in Figure 2 is fully capable of receiving any signal its inputs including a differential input signal (D1, D2). Clearly, when the circuit of Dillon receives a differential input signal at its inputs (D1, D2), then the circuits 65 and 66 in Figure 2 will generate a differential output signal at PAD1 and PAD2. Note that Dillon also discloses that in successive response to Vdd and ground signals from the multiplex 70, successive output signals at output ports 21 and 22 will have substantially Vdd and ground signal levels (Col. 3, lines 37-42), so the signals at ports 21 and 22 are also differential signal.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Thursday from 8:00am to 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LONG NGUYEN
PRIMARY EXAMINER